CLAIMS

1. A power up reset circuit, comprising:

a comparator having first and second inputs and an output;

at least one diode connected transistor coupled to the first input and to a power supply voltage;

at least one diode connected transistor or at least one resistor divider coupled to the second input and to ground; and

a reset signal generated at the output when the voltages at the first and second inputs are approximately the same.

2. The power up reset circuit of claim 1, wherein the at least one diode connected transistor coupled to the first input tries to maintain a one or more threshold voltage (Vt) difference from the power supply voltage at the first input.

3. The power up reset circuit of claim 1, wherein the at least one diode connected transistor or the at least one resistor divider coupled to the second input tries to maintain a one or more threshold voltage (Vt) difference from ground potential.

4. The power up reset circuit of claim 1, wherein a first plurality of diode connected transistors are coupled in series and coupled to the first input of the comparator.

5. The power up reset circuit of claim 4, wherein a second plurality of diode connected transistors are coupled in series and coupled to the second input of the comparator.

6. The power up reset circuit of claim 1, further comprising:

a hysteresis circuit coupled to the comparator, the hysteresis circuit configured to protect the power up reset circuit from glitches in the power supply voltage or the ground.

7. The power up reset circuit of claim 6, wherein the hysteresis circuit is further configured to lower a voltage level that the power supply voltage provides to the power up reset circuit in order to cause a change in the reset signal.

8. An integrated circuit having a power up reset circuit, comprising:

a power supply directly connected to a first resistor, the first resistor in series with a first input node and a first diode connected transistor, the first diode connected transistor connected to ground;

a second diode connected transistor directly connected to the power supply and connected in series with a second input node and a second resistor, wherein the second resistor is directly connected to ground;

a comparator connected to the first input node and second input node and producing a reset signal, when the voltages at the first and second input nodes are about equal.

9. The integrated circuit of claim 8, wherein the integrated circuit comprises a Field Programmable Gate Array (FPGA).

10. The integrated circuit of claim 8, wherein the comparator provides a two state output signal at the output, a first or high logic level output state or a second or low logic level output state.

11. The integrated circuit of claim 8, wherein the first diode connected transistor is connected directly to ground.

12. The integrated circuit of claim 8, wherein the reset signal is at an output node between a first capacitor connected to the power supply and a second capacitor connected to ground.

13. The integrated circuit of claim 8, further comprising a hysteresis circuit coupled to the comparator, the hysteresis circuit comprising a feedback transistor connected in parallel with a third resistor, wherein the gate of the feedback transistor is connected to the reset signal and wherein the third resistor is connected to the first diode connected transistor.

14. A method for providing a power up reset signal to an integrated circuit, the integrated circuit having a comparator with a first input and a second input and producing the power up reset signal, the method comprising the steps of:

a. a power supply voltage increasing to a predetermined supply voltage;

b. responsive to step a, causing the first input to increase in voltage to at least one diode threshold voltage above ground potential;

c. responsive to step a, causing the second input to increase in voltage to at least one diode threshold voltage below the power supply voltage; and

d. generating the power up reset signal, when the voltage levels at the first and second inputs of the comparator are approximately the same.

15. The method of claim 14, wherein the generating the power up reset signal comprises causing the power up reset signal to transition from a high logic level to a low logic level.

16. The method of claim 15, further comprising the step of: changing a voltage trip point, comprising when the voltage

levels at the first and second inputs of the comparator are approximately the same, after the power up reset signal has been generated.

17. The method of claim 14, further comprising the steps of:

unasserting an enable signal to the comparator so that the comparator does not consume any static current.

18. The method of claim 14, wherein the integrated circuit comprises a Programmable Logic Device (PLD).